Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A device comprising:

an MPEG decoder structured to decode several coded images from at least a first and a second MPEG stream for displaying simultaneously one image of the first MPEG stream and one image of the second MPEG stream, the coded images belonging to a first type or to a second type, the images of the first type being frame interlaced images comprising two fields, the decoding of which is completed in two periods, one of the periods being equal to the time duration of one field display, and the images of the second type being interlaced half-images or progressive images, the decoding of which is completed in one of the periods; and

a decoder control circuit for controlling the MPEG decoder, the decoder control circuit being configured to receive an order to decode a plurality of images at each of the periods and including a priority assignment circuit structured to, at each period, grant among the images to be decoded a decoding priority such that the highest decoding priority is granted to images of the first ~~typethat~~ type that have received their decoding order for more than one of the periods, a lower decoding priority is granted to images of the second type, and the lowest decoding priority is granted to images of the first type that have received their decoding order for less than one of the periods.

2. (Original) The device according to claim 1, wherein the decoder control circuit further includes a pointer memory for storing the beginning addresses of each of the images to be displayed.

3. (Original) The device according to claim 1, wherein said decoder control circuit further includes a safety circuit for adding a predetermined header before each image

provided to the decoder so that two images put end to end cannot form a code that causes a malfunction of the decoder.

4. (Canceled)

5. (Original) The device according to claim 1, further comprising:

a memory that stores coded data and decoded data;

a first bus that connects the decoder control circuit to the memory;

a display control circuit connected between a screen and the first bus; and

a microprocessor connected by a second bus to the decoder control circuit and the display control circuit.

6.-7. (Canceled)

8. (Previously Presented) A method for prioritizing MPEG images to be decoded by a single MPEG decoder, the method comprising:

receiving first and second image sequences of coded images from more than one MPEG stream, each coded image having a frame interlaced image type or an interlaced half-image image type;

receiving a stream of decoding commands in a series of synchronizing periods, each decoding command corresponding to a respective one of the coded images;

adding each decoding command to a priority list;

prioritizing the decoding commands by assigning to each decoding command a priority level based on the image type of the coded image corresponding to the decoding command and the period in which the decoding command was received;

decoding the coded images in a priority order based on the priorities assigned to the coded images, thereby producing first and second images sequences of decoded images; and

displaying the first and second image sequences.

9. (Previously Presented) The method according to claim 8 wherein prioritizing the decoding commands comprises:

assigning a higher priority to a first decoding command corresponding to a frame interlaced coded image than to a second decoding command corresponding to a interlaced half-image coded image if the second decoding command has been on the list for less than one synchronizing period and otherwise assigning a higher priority to the second decoding command than to the first decoding command.

10. (Previously Presented) A method for decoding a plurality of MPEG sequences from more than one MPEG stream simultaneously using a single MPEG decoder, the method comprising:

receiving a first sequence of frame-interlaced coded images and a second sequence of non-frame-interlaced coded images;

receiving a stream of decoding commands, each decoding command corresponding to a respective one of the coded images;

prioritizing the received coded images based on whether the coded image is a frame-interlaced coded image and on when the corresponding decoding command was received;

decoding the coded images using the single MPEG decoder based on the prioritizing, thereby producing decoded images of first and second images sequences; and

saving the decoded images.

11. (Original) The method according to claim 10 wherein the decoding commands are received in a series of synchronizing periods and prioritizing the coded images includes, during each synchronizing period, prioritizing the decoding commands received in the synchronizing period.

12. (Original) The method according to claim 11 wherein prioritizing the coded images includes, during each synchronizing period, assigning a lower priority to the

decoding command received during the synchronizing period than to any decoding command received in a prior synchronizing period.

13. (Previously Presented) The method according to claim 11 wherein the coded images of the first sequence are decoded during the synchronizing period in which the decoding commands corresponding to the coded images of the first sequence are received and the coded images of the second sequence are decoded during a synchronizing period subsequent to the synchronizing period in which the decoding commands corresponding to the coded images of the second sequence are received.

14. (Previously Presented) The method according to claim 11 wherein prioritizing the coded images includes:

assigning a higher priority to a first coded image than to a second coded image if the decoding command corresponding to the first coded image was received in a synchronizing period prior to the synchronizing period in which the decoding command corresponding to the second coded image was received.

15. (Canceled)

16. (Previously Presented) The method according to claim 14, wherein the second sequence comprises a sequence of interlaced half-images.

17. (Original) The method according to claim 10 wherein the coded images are read from a memory device and the decoded images are saved to the memory device.

18. (Previously Presented) A device, comprising:

an MPEG decoder configured to decode a plurality of MPEG image sequences from more than one MPEG stream in parallel; and

a controller coupled to the MPEG decoder and configured to control the MPEG decoder such that:

a received frame-interlaced image sequence is decodable during two periods following an associated decoding order; and

a received non-frame-interlaced image sequence is decodable during a first period following an associated decoding order.

19. (Previously Presented) The device of claim 18 wherein the controller comprises a prioritizing module configured to assign a decoding priority to received frame-interlaced image sequences that are not decoded in a first period following their associated decoding order.

20. (Previously Presented) The device of claim 18, wherein the controller comprises a pointer memory to store images sequences to be decoded and associated decoding parameters and the controller assigns a decoding priority to received image sequences based at least in part on the associated decoding parameters.

21. (Previously Presented) The device of claim 18 wherein the received image sequences of the first type are interlaced complete-image sequences and the received image sequences of the second type are interlaced half-image sequences.

22. (Previously Presented) The device of claim 18 wherein the controller comprises a prioritizing module configured to assign a first decoding priority to received frame-interlaced image sequences during a second period following their associated decoding order, a second decoding priority to received non-frame-interlaced image sequence and a third decoding priority to received frame-interlaced image sequence during a first period following their associated decoding order.

23. (Previously Presented) The device of claim 18 wherein the controller comprises means for assigning a decoding priority to received image sequences.

24. (Previously Presented) The device of claim 18 wherein the controller is further configured to control the MPEG decoder such that a first decoded image sequence of a coded image from a first MPEG stream is produced and a second decoded image sequence of a coded image from a second MPEG stream is produced.

25.-26. (Canceled)

27. (Previously Presented) The method of claim 10 wherein the first decoded image sequence is a decoded image sequence from a first MPEG stream and the second decoded image sequence is a decoded image sequence a second MPEG stream.

28. (Previously Presented) The method according to claim 14, wherein the second sequence comprises a sequence of non-interlaced complete images.

29. (New) The method of claim 8 wherein prioritizing the decoding commands includes:

assigning a first priority level to a first decoding command received during a preceding synchronization period and corresponding to a frame interlaced coded image type;

assigning a second priority level, lower than the first priority level, to a second decoding command corresponding to an interlaced half-image coded image type; and

assigning a third priority level, lower than the second priority level, to a third decoding command received during a current synchronization period and corresponding to the frame interlaced coded image type.

30. (New) The method of claim 10 wherein prioritizing the coded images includes:

assigning a first priority level to a first decoding command received during a preceding synchronization period and corresponding to the first sequence of frame-interlaced coded images;

assigning a second priority level, lower than the first priority level, to a second decoding command corresponding to the second sequence of non-frame-interlaced coded images; and

assigning a third priority level, lower than the second priority level, to a third decoding command received during a current synchronization period and corresponding to the first sequence of frame-interlaced coded images.

31. (New) The device of claim 22 wherein the first decoding priority is higher than the second decoding priority and the second decoding priority is higher than the third decoding priority.